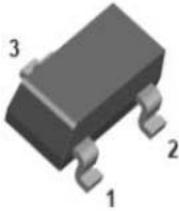
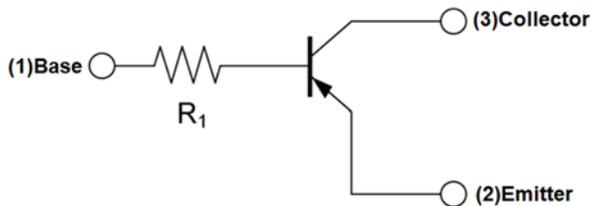


PNP Digital Transistors (Built-in Resistors)



SOT-23



Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for automatic insertion

Application

- Signal amplification
- Switching circuit

Mechanical data

- **Package:** SOT-23
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102

■ Maximum Ratings ($T_a=25^\circ\text{C}$ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Device marking code				94
Collector-base voltage	V_{CBO}	V		-50
Collector-emitter voltage	V_{CEO}	V		-50
Emitter-base voltage	V_{EBO}	V		-5
Collector current	I_C	mA		-100
Power dissipation	P_D	mW		200
Operation junction temperature	T_J	$^\circ\text{C}$		-55 to +150
Storage temperature	T_{STG}	$^\circ\text{C}$		-55 to +150



DTA114TCA

RoHS
COMPLIANT

■ Electrical Characteristics (T_a=25°C Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Collector-base voltage	V _{CBO}	V	I _C =-50μA	-50		
Collector-emitter voltage	V _{CEO}	V	I _C =-1mA	-50		
Emitter-base voltage	V _{EBO}	V	I _E =-50μA	-5		
Collector-base cut-off current	I _{CBO}	μA	V _{CB} =-50V			-0.5
Emitter-base cut-off current	I _{EBO}	μA	V _{EB} =-4V			-0.5
DC current gain	h _{FE}		V _{CE} =-5V, I _C =-1mA	100		600
Input resistance	R _i	kΩ		7	10	13
Collector-emitter saturation voltage	V _{CE(sat)}	V	I _C =-10mA, I _B =-1mA			-0.3
Transition frequency	f _T	MHz	V _{CE} =-10V, I _E =5mA, f=100MHz		250	

■ Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	R _{θJ-A} ⁽¹⁾	°C/W	625
Thermal resistance, junction-to-case	R _{θJ-C} ⁽¹⁾	°C/W	500

Note:

(1) Device mounted on PCB, single-sided copper, with standard footprint

■ Ordering Information

Preferred P/N	Packing code	Unit weight(g)	Minimum package(pcs)	Inner box quantity(pcs)	Outer carton quantity(pcs)	Delivery mode
DTA114TCA	F2	Approximate 0.009	3000	30000	120000	7" reel



■ Characteristics

Fig 1: Static Characteristics

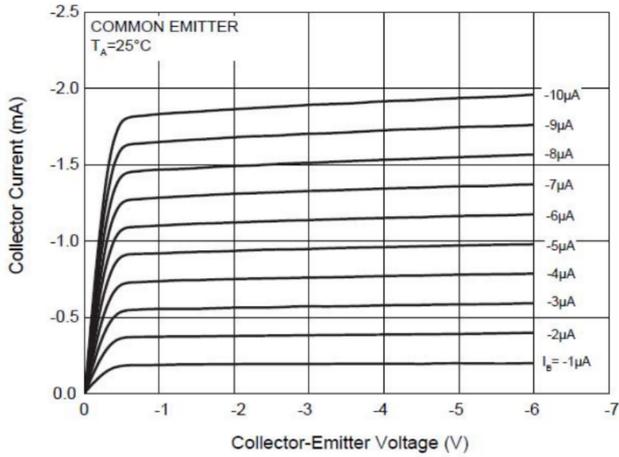


Fig 2: DC Current Gain Characteristics

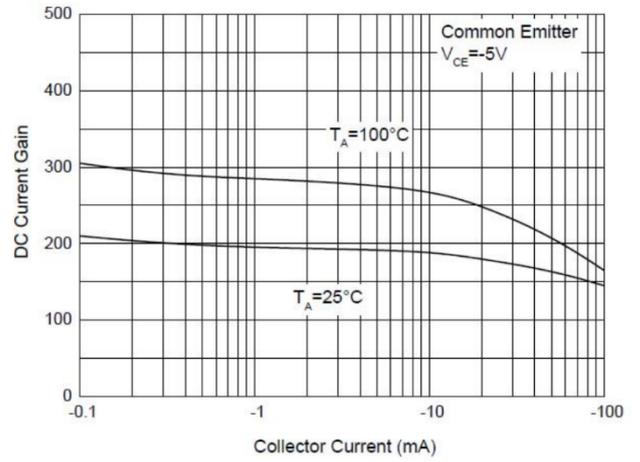


Fig 3: Output Voltage Characteristics

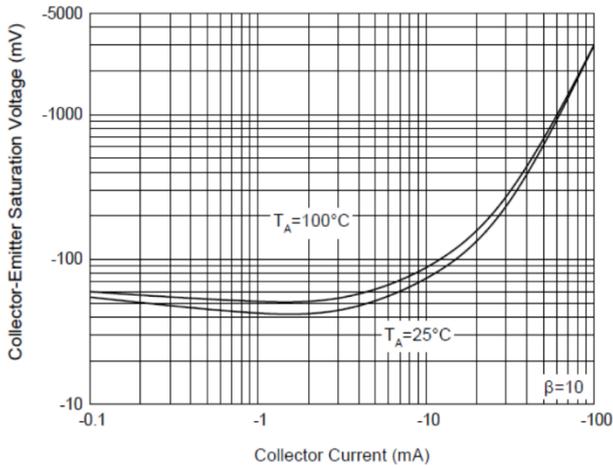
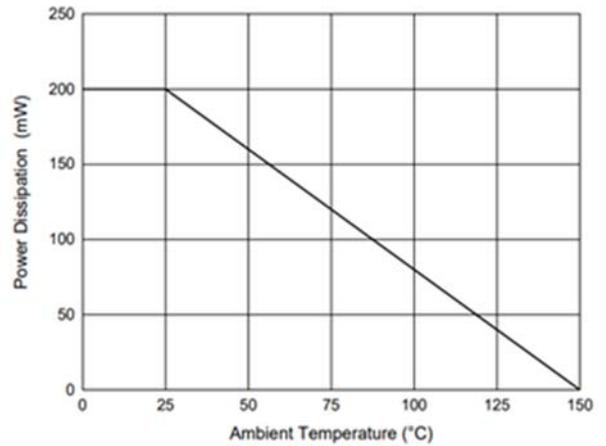
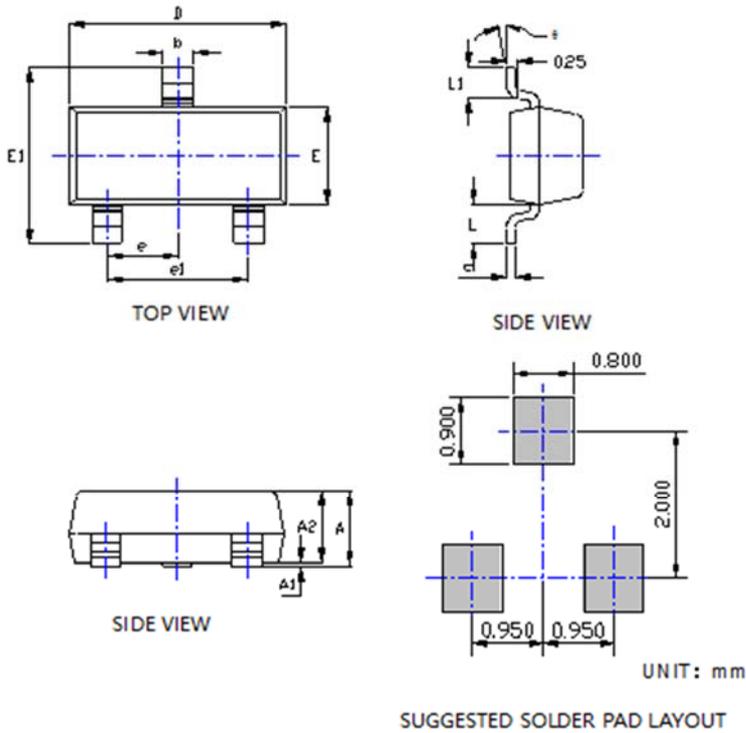


Fig 4: P_D - T_a Curve



■ Outline Dimensions



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
φ	0°	8°	0°	8°

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位, 除非另有说明]
2. General tolerances: ±0.10mm unless otherwise specified.
[通用公差为±0.10mm, 除非另有说明]
3. Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
4. All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
5. Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
6. Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸, 不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺, 但是包含了包封错位的最大尺寸]
7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面, 共面性最大为0.1mm]
8. ★It is the key size.
[★ 标记为关键尺寸]



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